Machine translation JP2004191574

(19)**Publication country**Japan Patent Office (JP)
(12)**Kind of official gazette**A publication of patent applications (A)
(11)**Publication No.**JP,2004-191574,A (P2004-191574A)
(43)**Date of Publication**Heisei 16(2004) July 8 (2004.7.8)
(54)**Title of the Invention**An electrooptics panel, a scanning line driving circuit, a data line driving circuit, an electronic device, and a drive method of an electrooptics panel
(51)**The 7th edition of International Patent Classification**
G09G 3/36
G02F 1/133
G09G 3/20
H05B 33/14
FI
G09G 3/36
G02F 1/133 550
G09G 3/20 611 A
G09G 3/20 621 B
G09G 3/20 623 F
G09G 3/20 623 H
G09G 3/20 623 L
G09G 3/20 624 B
G09G 3/20 631 R
G09G 3/20 641 C
G09G 3/20 641 G
G09G 3/20 641 P
G09G 3/20 650 M
G09G 3/20 660 U
H05B 33/14 A

Request for Examination Unrequested
The number of claims 12
Mode of ApplicationOL
Number of Pages21
(21)**Application number**Application for patent 2002-358380 (P2002-358380)
(22)**Filing date**Heisei 14(2002) December 10 (2002.12.10)
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Theme code (reference)
2H093

3K007

5C006

5C080

F-term (reference)

2H093 NA16 NA53 NA54 NA80 NC03 NC10 NC13 NC15 NC16 NC28 NC29 NC34 NC59 ND49 ND50

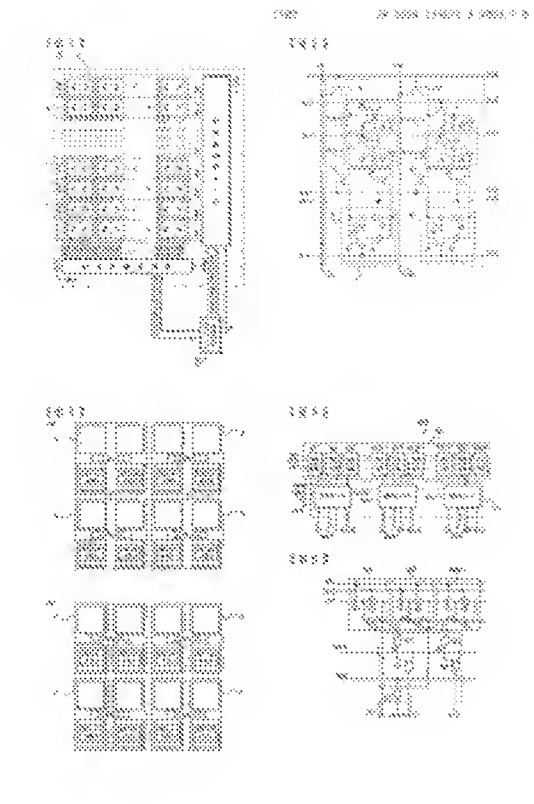
3K007 AB17 BA06 DB03 GA04

5C006 AA02 AA09 AA12 AA16 AA22 AC27 AC28 AF05 AF36 AF68 AF69 AF83 BB16 BC12 BC20 BF03 BF11 BF26 BF27 EB05 FA04 FA44 FA47 FA 56

5C080 AA06 AA10 BB05 CC03 DD22 DD26 EE26 EE27 EE28 FF11 HH09 JJ02 JJ03 JJ04 JJ06 KK04 KK07

Abstract:

PROBLEM TO BE SOLVED: To provide an electro-optical panel where the occupancy area of a memory is reduced.SOLUTION: A main pixel P is provided with four sub-pixels Ps, memories Ma and Mb and TFT 50, 60 and 61. In a first mode, the TFT 51 and 54 of the sub-pixels Ps are successively turned on in a period in which the TFT 50 is turned on, and signals Sm and Sm+1 are written. On the other hand, in a write-in period in a second mode, the TFT 50 and 60 are turned on, and signals Sm and Sm+1 are written in memories Ma and Mb. In a read-out period, the TFT 60 and 61 are alternately turned on, and the storage contents of the memories Ma and Mb are written in the sub-pixels Ps.



JPO Machine translation abstract:
(57)**Abstract**
SUBJECT A memory is shared between sub pixels.
Means for Solution The main pixel P is provided with TFT50, and 60 and 61. **the four sub pixels Ps, the memories Ma and Mb(s) and** In the 1st mode, one by one a period **one / a period / TFT50** , and signal Sm and Sm+1 is written in. **TFT51 of the sub pixel Ps, and 54** On the other hand, if it is in a write period in the 2nd mode, and signal Sm and Sm+1 is written in the memory Ma and Mb. **TFT50 and 60** By turns, and the memory Ma and a memory content of Mb are written in the sub pixel Ps. **during the read-out TFT60 and 61**
Chosen drawing Drawing 2

Claim(s)
Claim 1
Have a sub pixel provided corresponding to intersection of a scanning line, two or more data lines, and two or more said scanning lines and said data lines, and a main pixel which has said two or more sub pixels, and said main pixel, The number of said sub pixels which are provided with one or more memories which memorize image data of M (M is natural number) bit, and are matched with per said memory is a drive method of an electrooptics panel exceeding 1,
In the 1st mode, gradation of N bit is displayed on said each sub pixel based on image data of N (N>=M and N are natural numbers) bit,
In the 2nd mode, while memorizing image data of M bit in said each memory, gradation of M bit is displayed on said sub pixel matched with said each memory.
A drive method of an electrooptics panel characterized by things.
Claim 2
In said 1st mode, a signal generated based on image data of N bit is written in said each

sub pixel,
In said 2nd mode, image data of M bit is memorized in said memory, and gradation of M bit is displayed in common with said sub pixel connected to the memory concerned based on image data read from said memory.
A drive method of an electrooptics panel characterized by things.

Claim 3

A drive method of an electrooptics panel which said M bit is 1 bit and is characterized by displaying gradation of each of said sub pixel in binary in said 2nd mode.

Claim 4

Said memory can output selectively data and inversion data which reversed this.
A drive method of the electrooptics panel according to claim 3 reading said data and said inversion data from said memory with a given period, and supplying said sub pixel.

Claim 5

Two or more scanning lines,
Two or more data lines,
A sub pixel provided corresponding to intersection of said scanning line and said data line,
It has a main pixel which has said two or more sub pixels,
Said main pixel is provided with one or more memories which memorize image data of M (M is natural number) bit, and the number of said sub pixels matched with per said memory exceeds 1.
An electrooptics panel characterized by things.

Claim 6

Said main pixel,
Said data line and one input/output terminal are connected, and an input/output terminal of another side is provided with the 1st switching element connected with wiring,
Said wiring connects said one or more sub pixels corresponding to said memory.
The electrooptics panel according to claim 5 characterized by things.

Claim 7

The electrooptics panel according to claim 6, wherein said main pixel is provided with a switching means established between said memory and said wiring.

Claim 8

Said switching means is provided with the 2nd switching element and the 3rd switching element,
Said memory,
Capacity to which said 2nd switching element and one terminal are connected,
The 1st inverting circuit where one terminal and input terminal of said capacity are connected,
The 2nd inverting circuit where an input terminal is connected to said 3rd switching element and an output terminal of said 1st inverting circuit,
The 4th switching element provided between an output terminal of said 2nd inverting circuit, and one terminal of said capacity
The electrooptics panel according to claim 7 characterized by preparation ******.

Claim 9

It is an electrooptics panel given in any 1 clause among Claims 5-8 constituting from said a part of two or more sub pixels.

Claim 10

It is a scanning line driving circuit which drives the electrooptics panel according to claim 8,
In the 1st mode, said 1st switching element of said main pixel is made into an ON state one by one via a scanning line, and said sub pixel contained in the main pixel concerned is chosen one by one along said scanning line in the "on" period concerned,
In a write period in the 2nd mode, said 1st switching element is made into an ON state one by one via said scanning line, In the "on" period concerned, said 2nd switching element is controlled via said scanning line to make an ON state and said 3rd switching element into an OFF state, and to make said 4th switching element into an OFF state,
In a read-out period in the 2nd mode, it controls via said scanning line to turn an OFF state on and off for said 1st switching element, and to make an ON state, said 2nd

switching element, and said 3rd switching element turn said 4th switching element on and off exclusively with a given period.
A scanning line driving circuit characterized by things.

Claim 11

It is a data line driving circuit which drives an electrooptics panel of a description in any 1 clause among Claims 5-9,
It has a means to generate a sampling pulse which shifts a start pulse according to a clock signal, and becomes active exclusive one by one,
While sampling respectively a picture signal which obtained image data of said N bit by changing it into an analog signal in the 1st mode based on said sampling pulse and supplying said data line one by one, In a write period in said 2nd mode, if image data of said M bit is respectively sampled based on said sampling pulse, said data line is supplied one by one and it is in a read-out period in the 2nd mode, operation is suspended.
A data line driving circuit characterized by things.

Claim 12

An electronic device which equipped any 1 clause with an electrooptics panel of a description among Claims 5-9.

Detailed Description of the Invention

0001

Field of the Invention

This invention relates to the electrooptics panel etc. which equipped the pixel with the memory function.

0002

Description of the Prior Art

The liquid crystal panel of an active matrix is provided with the liquid crystal with which it filled up between the element substrate by which the switching element was mainly provided in each of the picture element electrode arranged to matrix form, the counter substrate in which the light filter etc. were formed, and these both boards. In such composition, if a scanning signal is impressed to a switching element via a scanning line, the switching element concerned will be in switch-on. If a picture signal is impressed to a picture element electrode via the data line in the case of this switch-on, a predetermined electric charge will be accumulated in the liquid crystal layer between the picture element electrode concerned and a counterelectrode (common electrode).

0003

In such a liquid crystal panel, the light transmittance of a liquid crystal changes according to impressed electromotive force. By changing the voltage written in liquid crystal capacity, the voltage gradient method on which gradation is displayed is well-known. On the other hand, one pixel is divided into two or more sub pixels, and the area gradation method for realizing a gradation display by giving an on-off indication of these sub pixels is known (for example, patent documents 1).

0004

The liquid crystal device provided with the mode in which the gradation display by an area gradation method is performed according to the data which provided one memory in one sub pixel, and was memorized, and the mode in which a gradation display is performed by a voltage gradation method is also known (for example, patent documents 2).

0005

Patent documents 1

JP,2001-281628,A (drawing 2 and drawing 3)

0006

Patent documents 2

JP,2002-22957,A (Claim 1 and drawing 4)

0007

Problem to be solved by the invention

By the way, it is needed that the occupation area of a memory is small for the luminosity

of an electrooptics panel being influenced by the numerical aperture and raising a numerical aperture. However, since one memory was arranged at one sub pixel if it was in the conventional electrooptics panel, there was a problem that a display image became dark.

0008

This invention is made in view of the situation mentioned above, and makes it solution SUBJECT to provide the electrooptics panel which decreased the occupation area of the memory etc.

0009

Means for solving problem

In order to solve an aforementioned problem, the drive method of the electrooptics panel concerning this invention, Have the sub pixel provided corresponding to intersection of a scanning line, two or more data lines, and two or more said scanning lines and said data lines, and a main pixel which has said two or more sub pixels, and said main pixel, It has one or more memories which memorize the image data of M (M is natural number) bit, The number of said sub pixels matched with per said memory is 1 how to drive the electrooptics panel which exceeds, and in the 1st mode. Based on the image data of N (N>=M and N are natural numbers) bit, display the gradation of N bit on said each sub pixel, and in the 2nd mode. While memorizing the image data of M bit in said each memory, the gradation of M bit is displayed on said sub pixel matched with said each memory.

0010

According to this invention, in the 1st mode, a high definition picture can be displayed and a picture with low resolution and gradation number can be displayed in the 2nd mode as compared with the 1st mode. When displaying Still Picture Sub-Division, it becomes unnecessary to rewrite the memory content of a memory, since the 2nd mode serves as a display which used the memory function. Therefore, since a scanning line and the data line are chosen one by one and it becomes unnecessary to drive them, it becomes possible to reduce power consumption substantially.

0011

In said 1st mode, write here the signal generated based on the image data of N bit in said each sub pixel, and in said 2nd mode. It is preferred to display the gradation of M bit in common with said sub pixel connected to the memory concerned based on the image data which memorized the image data of M bit in said memory, and was read from said memory. In this case, in the 2nd mode, although the sub pixel connected to a certain memory will display the gradation of M bit, since the main pixel can have two or more memories, the gradation display of it by an area gradation method is attained.

0012

Said M bit is 1 bit and it is preferred to display the gradation of each of said sub pixel in binary in said 2nd mode. According to this invention, structure of a memory is made simple and it becomes possible to perform image display in the 2nd mode by easy control.

0013

It adds, and it is possible to output selectively data and inversion data which reversed this, and, as for said memory, it is desirable to read said data and said inversion data from said memory with a given period, and to supply said sub pixel. To use a liquid crystal as electrooptic material, it is necessary to carry out the alternating current drive of the liquid crystal from a viewpoint which prevents a printing phenomenon. According to this invention, in the 2nd mode, since it becomes possible to reverse voltage read from a memory focusing on reference level, the alternating current drive of the liquid crystal can be carried out.

0014

An electrooptics panel concerning this invention Next, two or more scanning lines and two or more data lines, Have a sub pixel provided corresponding to intersection of said scanning line and said data line, and a main pixel which has said two or more sub pixels, and said main pixel, It has one or more memories which memorize image data of M (M is natural number) bit, and the number of said sub pixels matched with per said memory exceeds 1. According to this invention, since the number of said sub pixels matched with

per memory exceeds 1, area of a memory occupied to a viewing area is reducible. Since a memory area does not contribute to a penetration of light, it can raise a numerical aperture by reducing occupation areas. As a result, it is bright and, moreover, an electrooptics panel with little power consumption can be provided. If a certain memory is matched with one sub pixel, other memories are matched with two sub pixels, and are and it concludes as a whole that the number of sub pixels matched with per memory exceeds 1, a case where it is matched with one or more memories is included.

0015

Here, said data line and one input/output terminal are connected, the input/output terminal of another side is provided with the 1st switching element connected with wiring, and, as for said main pixel, it is **said wiring** preferred to connect said one or more sub pixels corresponding to said memory. This 1st switching element may be provided for every data line, and the 1st two or more switching element may be contained in one main pixel.

0016

As for said main pixel, it is preferred to have the switching means established between said memory and said wiring. By this switching means, a memory is separated and connected with a sub pixel.

0017

Said switching means is provided with the 2nd switching element and the 3rd switching element, and more specifically said memory, The 1st inverting circuit where the capacity to which said 2nd switching element and one terminal are connected, and one terminal and input terminal of said capacity are connected, It is preferred to have the 2nd inverting circuit where an input terminal is connected to said 3rd switching element and the output terminal of said 1st inverting circuit, and the 4th switching element provided between the output terminal of said 2nd inverting circuit and one terminal of said capacity.

0018

A main pixel may consist of said a part of two or more of said sub pixels. That is, only the portion (main picture element part) by which the 1st mode and the 2nd mode are applied into a viewing area, and the 1st mode are applied, and may carry out partial mixture. Although the screen which awaits a telephone call is displayed in a cellular phone, such a screen has a portion which displays an icon etc. on the upper part or the lower part. Then, low power consumption is realizable by arranging a main pixel into such a portion.

0019

Next, the scanning line driving circuit concerning this invention drives the electrooptics panel mentioned above, and in the 1st mode. In **make said 1st switching element of said main pixel into an ON state one by one via a scanning line, and** the "on" period concerned, In **choose said sub pixel contained in the main pixel concerned one by one along said scanning line, and** the write period in the 2nd mode, Said 1st switching element is made into an ON state one by one via said scanning line, In **in the "on" period concerned, control said 2nd switching element via said scanning line to make an ON state and said 3rd switching element into an OFF state, and to make said 4th switching element into an OFF state, and** the read-out period in the 2nd mode, It controls via said scanning line to turn an OFF state on and off for said 1st switching element, and to make an ON state, said 2nd switching element, and said 3rd switching element turn said 4th switching element on and off exclusively with a given period.

0020

According to this invention, in the 1st mode, each sub pixel can be chosen one by one, data is written in a memory and the write period in the 2nd mode enables it to read data and inversion data from a memory by turns, and to supply each sub pixel in the read-out period in the 2nd mode.

0021

Next, the data line driving circuit concerning this invention is used for the electrooptics panel mentioned above, Have a means to generate the sampling pulse which shifts a start pulse according to a clock signal, and becomes active exclusive one by one, and in the 1st mode. While sampling respectively the picture signal which obtained the image

data of said N bit by changing it into an analog signal based on said sampling pulse and supplying said data line one by one, In the write period in said 2nd mode, the image data of said M bit is respectively sampled based on said sampling pulse, said data line is supplied one by one, and if it is in the read-out period in the 2nd mode, operation is suspended. when a high definition display is required according to this data line driving circuit, while supplying the picture signal which can display the gradation of N bit to the data line -- low -- when a minute display is sufficient, since a read-out period suspends operation, it can reduce power consumption substantially by only the write period operating.

0022

Next, the electronic device concerning this invention is provided with the electrooptics panel mentioned above. For example, a view finder, a portable telephone, a notebook computer, a video projector, etc. which are used for a liquid crystal device and a video camera correspond.

0023

Mode for carrying out the invention

Hereafter, an embodiment of this invention is described with reference to Drawings.

<1. a 1st embodiment>

<1-1: Entire configuration **of a liquid crystal device** >

First, an electro-optic device concerning an embodiment of this invention is explained. This electro-optic device is a transmission type liquid crystal device which performs a predetermined display by that electrooptic change using a liquid crystal as electrooptic material. The main pixel P is constituted from the four sub pixels Ps by this liquid crystal device. And in the 1st mode, while writing voltage according to gradation in each sub pixel Ps and displaying a picture, in the 2nd mode, each sub pixel Ps is driven with a binary, and image display by an area gradation method is performed.

0024

Drawing 1 is a block diagram showing an entire configuration of a liquid crystal device concerning an embodiment. This liquid crystal device is provided with liquid crystal panel AA and the timing generating circuit 300. Liquid crystal panel AA is provided with the picture element region A, the scanning line driving circuit 100A, and the data line driving circuit 200 on the element substrate.

0025

Inputted-image-data D supplied to this liquid crystal device is the form of three bit parallels, for example. Synchronizing with inputted-image-data D, the timing generating circuit 300 The Y clock signal CKY, Reversal Y clock signal CKYB, X clock signal CKX, reversal X clock signal CKXB, the Y transfer starting pulse SPY, and X transfer starting pulse SPX are generated, and the scanning line driving circuit 100A and the data line driving circuit 200 are supplied.

0026

Here, the Y clock signal CKY specifies the period which chooses the scanning line 2, and reversal Y clock signal CKYB reverses the logical level of the Y clock signal CKY. X clock signal CKX specifies the period which chooses the data line 3, and reversal X clock signal CKXB reverses the logical level of X clock signal CKX.

0027

Next, as shown in drawing 1, while the scanning line 2 of a lot arranges in parallel and is formed in accordance with the direction of J group X by six, in accordance with the direction of Y, the data line 3 of K (K is two or more natural numbers) book arranges in the picture element region A in parallel, and is formed in it. And the sub pixel Ps is formed in near intersection of the scanning line 2 and the data line 3. Since the sub pixel Ps is specified **the following explanation** , when the number of Y ("Y" as shown a scanning line in drawing 1, when it expresses with 2-YV), and the data line is set to X ("X" as shown the data line in drawing 1, when it expresses with 3-X) for the group number item of a scanning line, The sub pixel corresponding to scanning line 2-Y2 shall be expressed with Ps (X, Y1), and the sub pixel corresponding to scanning line 2-Y3 shall be expressed with Ps (X, Y2).

0028

<1-2: Pixel configuration >

Drawing 2 is a circuit diagram showing detailed composition of the main pixel P formed corresponding to intersection with scanning line 2-n1 - 2-n6, data-line 3-m, and 3-m+1. As shown in this figure, the main pixel P is provided with the four sub pixels Ps (m, n1), Ps (m, n2), Ps (m+1, n1) and Ps (m+1, n2), TFT50, TFT60, TFT61 and the memory Ma, and Mb.

0029

The sub pixel Ps (m, n1) has TFT51, the storage capacitance 52, and the liquid crystal capacity 53. The liquid crystal capacity 53 is constituted by a picture element electrode, a counterelectrode, and liquid crystal with which it fills up among them. Other sub pixels Ps as well as the sub pixel Ps (m, n1) are constituted.

0030

A gate is connected to scanning line 2-n1, a source is connected to data-line 3-m, and, as for TFT50 of an upper left end, a drain is further connected to the sub pixels Ps (m, n1) and Ps (m, n2). In a write period of image data in a write period of a picture signal in the 1st mode, and the 2nd mode, TFT50 will be in an ON state, and will be in an OFF state in a display period. TFT50 is controlled by the scanning signal Gn supplied by scanning line 2-n1.

0031

TFT60 and 61 are used in order to control whether the sub pixels Ps (m, n1) and Ps (m, n2) are connected with the memory Ma. A gate of TFT60 is connected to scanning line 2-n4, the source is connected with a drain of TFT50, and the drain is further connected with the memory Ma. A gate of TFT61 is connected to scanning line 2-n5, the source is connected with a drain of TFT50, and the drain is further connected with the memory Ma. Turning on and off of TFT60 is controlled by signal Gmon1, and turning on and off of TFT61 is controlled by signal Gmon2.

0032

The memory Ma is provided with the capacity 62, the inverters 63 and 64, and TFT65. If one **TFT65** , latch circuitry will be formed by the inverters 63 and 64. Therefore, voltage of the capacity 62 will be held. On the other hand, since a loop is not formed if TFT65 turns off, it becomes possible to write voltage in the capacity 62. Therefore, if TFT65 is made one after writing voltage in the capacity 62, voltage written in the capacity 62 can be held. That is, the memory Ma functions as one bit memory. Turning on and off of TFT65 is controlled by the signal Gmrwn supplied via scanning line 2-n6. The signal Gmrwn points to writing of data with a low level, is high-level and directs read-out (maintenance) of data.

0033

While memorizing 1-bit data respectively in the memories Ma and Mb and controlling gradation of the sub pixel Ps (m, n1) and the sub pixel Ps (m, n2) by this example in the 2nd mode according to a memory content of the memory Ma, According to a memory content of the memory Mb, gradation of the sub pixel Ps (m+1, n1) and the sub pixel Ps (m+1, n2) is controlled. By this, the main pixel P becomes possible **displaying a gradient according to the number of the sub pixels Ps used as one** . If data specifically memorized by Da and the memory Mb in data memorized by the memory Ma is set to Db, and white shall be displayed for black at the time of 0 when said data is 1, By Da=Db=1, in black and remaining two sub pixels, the four sub pixels Ps serve as **the two sub pixels Ps** white by black, Da=1, Db=0 or Da=0, and Db=1 white and Da=Db=0, and a display of 3 gradation of the four sub pixels Ps is attained.

0034

Although 1-bit data was memorized to the memory Ma and Mb, it may be made to memorize data of M bit in a memory in an example shown in drawing 2, as shown in drawing 3 (A). Here, if the number of bits of inputted-image-data D is set to N, it will become N>=M (N and M are natural numbers). That is, in the 1st mode, N fatbits uses each sub pixel Ps (gradation is displayed 2^N), and M fatbits makes it a sub pixel (this example two pieces) connected with one memory in the 2nd mode. Although the main pixel P in drawing 3 (A) contained the four sub pixels Ps, the main pixel P which contains the two sub pixels Ps as shown in drawing 3 (B) may be assumed.

0035

Although resolution and a display gradient deteriorate as compared with the 1st mode,

since the display in the 2nd mode has memorized gradation to the memory Ma and Mb, it does not need to scan each sub pixel Ps and does not need to write in a picture signal. Therefore, since it becomes unnecessary to operate the scanning line driving circuit 100A and the data line driving circuit 200 synchronizing with a clock signal, it becomes possible to reduce power consumption substantially. In particular, in portable electronic devices, such as a portable telephone and PDA, there is a period which shows the menu screen provided with two or more icons. As compared with the case where video is displayed, low performance is sufficient for resolution and a display gradient required in order to display such a menu screen. Therefore, it becomes possible to long-time-ize time to operate with a battery, without spoiling the imaging quality seen from the user by displaying a menu screen etc. in the 2nd mode.

0036

<1-3: Composition **of a scanning line driving circuit** >

Drawing 4 is a block diagram showing the composition of the scanning line driving circuit 100A, and drawing 5 is a circuit diagram showing the composition of unit shift circuit Ua2n-1 of the scanning line driving circuit 100A - Ua2n+1, and Logical unit Ubn. As shown in these figures, the scanning line driving circuit 100A is provided with the shift register 110, the logic circuit group 120, and the inverter 130.

0037

The shift register 110 is provided with unit shift circuit Ua1 **2J+1 piece** - Ua2J+1, shifts the Y transfer starting pulse SPY one by one synchronizing with the Y clock signal CKY and reversal Y clock signal CKYB, and outputs a shift signal respectively. Unit shift circuit Ua1 - Ua2J+1 are provided with the clocked inverters 111 and 112 and the inverter 113. In unit shift circuit Ua2n-1, the Y clock signal CKY becomes high-level and active, and the clocked inverter 111 becomes high-level **inversion clock signal CKYB** and active **the clocked inverter 112** . If the Y clock signal CKY is in a period of high level, the Y transfer starting pulse SPY is outputted as a shift signal via the clocked inverter 111 and the inverter 113. On the other hand, latch circuitry is formed by the clocked inverter 112 and the inverter 113 in a period when inversion clock signal CKYB is high-level. Therefore, a logical level of a shift signal is held an applicable time limit. As a result, as for a shift signal outputted from a unit shift circuit, active period length of adjacent signals becomes that with which only a half cycle of the Y clock signal CKY lapped.

0038

The logic circuit group 120 is provided with J Logical unit Ub1-UbJ. Each Logical unit Ub1-UbJ supports the three unit shift registers Ua. n-th Logical unit Ubn corresponds to 2n - the 1st unit-shift-registers Ua2n-1 and 2n position unit-shift-registers Ua2n, and unit-shift-registers Ua2n+1 **2n+1 position** . Each Logical unit Ub1-UbJ is respectively provided with NAND circuits 121-125.

0039

<1-4: Composition **of a data line driving circuit** >

Drawing 6 is a circuit diagram showing composition of the data line driving circuit 200. As shown in this figure, the data line driving circuit 200 is provided with the shift register 210, the selection-circuitry group 220, DA converter 230, the digital buffer 240, the switches 231, 232, 241, and 242, and the signal wire 250.

0040

The shift register 210 is provided with K+1 unit shift circuit Uc1 - UcK+1, shifts X transfer starting pulse SPX one by one synchronizing with X clock signal CKX and reversal X clock signal CKXB, and outputs shift signal Gc1 - GcK+1 respectively. Unit shift circuit Uc1 - UcK+1 are provided with the clocked inverters 211 and 212 and the inverter 213. Since this composition is the same as that of the shift register 110 of the data line driving circuit 100, explanation is omitted.

0041

The selection-circuitry group 220 is provided with the K selection units Ud1-UdK. Each selection units Ud1-UdK are provided with NAND circuit 221, the inverter 222, and the sampling switch 223. The signal with which active period length lapped only the half cycle of X clock signal CKX is supplied to NAND circuit 221 from each unit shift circuit Uc1-UcK+1. Therefore, active period length is a half cycle of X clock signal CKX, and the sampling signals SP1-SPK become active exclusively.

0042
While the signal Gmem becomes high-level in the write period in the 2nd mode, it is set to a low level in the read-out period in the 1st mode and the 2nd mode. In the period of a low level, the switches 241 and 242 will be in an OFF state, while the signal Gmem will be in an ON state in a high-level period. The switches 231 and 232 are constituted so that turning on and off may change as exclusively as the switches 241 and 242.
0043
Therefore, when the signal Gmem directs the write period in the 2nd mode, as shown in a figure, the switches 241 and 242 will be in an ON state, and image data D is supplied to the signal wire 250 via the digital buffer 240. On the other hand, when the signal Gmem directs the 1st mode, a picture signal is supplied to the signal wire 250 via DA converter 230.
0044
<1-5: Operation **of a liquid crystal device** >
<1-5-1: 1st mode >
There are the 1st mode in which the display by a picture signal is performed, and the 2nd mode in which the display by image data is performed in the operating state of a liquid crystal device. The timing chart of the various signals in the 1st mode is shown in drawing 7. The memories Ma and Mb are not used in the 1st mode. For this reason, the signals Gmon1 and Gmon2 serve as a low level, and the sub pixel Ps and the memories Ma and Mb which are shown in drawing 2 are separated.
0045
Only the half cycle of the Y clock signal CKY is delayed, and the signal C1 is outputted by the unit shift circuit U2n as the signal C2. NAND circuit 121 reverses and outputs a logical product with signal C2B which reversed the signal C1 and the signal C2. For this reason, the signal C4 serves as a low level in **T2** the first half of the period T1 which becomes active **the signal C1** . NAND circuit 122 reverses and outputs the logical product of the signal C2 and the signal C3B. Therefore, the signal C5 serves as a low level by T3 during the second half of the period T1.
0046
On the other hand, NAND circuits 123 and 124 reverse and output the signals C4 and C5, when the signal Gmenb is a low level. Since the signal Gmenb becomes high-level in the 1st mode, in the period T2 and period T3, signal Gn-1 and signal Gn-2 which are outputted from NAND circuits 123 and 124 are respectively set to high level (active). Since the signal Gmem has a low level in the 1st mode, the signal Gmrwn outputted from NAND circuit 125 becomes high-level.
0047
Drawing 8 is a key map showing the course of the picture signal in period T3 shown in drawing 7. Since the scanning signal Gn and Gn-2 become active if it is in period T3, as shown in drawing 8, TFT50 and TFT54 will be in an ON state. Therefore, sampling signal Sm will be written in the sub pixel Ps (m, n2), and sampling signal Sm+1 will be written in the sub pixel Ps (m+1, n2).
0048
In the 1st mode, since the switches 231 and 232 shown in drawing 6 will be in an ON state, sampling signal Sm and Sm+1 becomes an analog signal which shows gradation. Therefore, the voltage according to gradation will be impressed to storage capacitance and liquid crystal capacity. And after period T3 is completed, TFT50 and TFT54 will be in an OFF state, and the voltage impressed to the storage capacitance 52 and the liquid crystal capacity 53 will be held. Thereby, image display becomes possible.
0049
<1-5-2: 2nd mode >
Next, it divides and explains during **which reads data** the read-out from the write period which writes in the data to the memories Ma and Mb for operation of the liquid crystal device in the 2nd mode, and them. Drawing 9 is a timing chart which shows operation of the liquid crystal device in the write period in the 2nd mode.
0050
In a write period, since the signal Gmemb serves as a low level, signal Gn-1 and Gn-2 which are the output signals of NAND circuits 123 and 124 become always high-level.

Although the signal Gmem is supplied to NAND circuit 125, since it is set to the signal Gmem being high-level in a write period, the signal Gmrwn becomes what reversed a logical product of the signal C1 and the signal C2. Therefore, the signal Gmrwn serves as a low level in period T3.

0051

Drawing 10 is a key map showing a course of a picture signal in period T3 shown in drawing 9. Since the scanning signal Gn, Gn-1, and Gn-2 become active and also signal Gmon1 becomes active if it is in period T3, as shown in drawing 10, TFT50, TFT51, TFT54, and TFT60 will be in an ON state. Therefore, signal Sm is written in the sub pixel Ps (m, n1), Ps (m, n2), and the memory Ma, and signal Sm+1 is written in the sub pixel Ps (m+1, n1), Ps (m+1, n2), and the memory Mb. Since signal Gmon2 and the signal Gmrwn serve as a low level in period T3, TFT61 and 65 will be in an OFF state. For this reason, voltage from which a logical level differs via TFT65 is not written in the capacity 62.

0052

Drawing 11 is a timing chart which shows operation of the liquid crystal device in the read-out period in the 2nd mode. First, in the read-out period in the 2nd mode, the Y clock signal CKY serves as a low level, and the Y transfer starting pulse SPY is not supplied to the scanning line driving circuit 100A. Therefore, the shift register 110 does not operate. For this reason, the signals C1 and C2 serve as a low level, and signal C2B, C3B, C4, and C5 become high-level. Since the signal Gmemb serves as a low level, it is set to signal Gn-1 and Gn-2 being high-level.

0053

Next, since the signal Gmrwn reverses the logical product of the signal C1, C2, and Gmem, it becomes high-level. In the example shown in drawing 11, the signals Gmon1 and Gmon2 are reversed with the 1 field period 1V. This is for exchange-izing voltage impressed to a liquid crystal. An inversion cycle may be an integral multiple of 1 horizontal scanning cycle.

0054

Drawing 12 is a key map showing the course of the picture signal in the period T4 shown in drawing 11. If it is in the period T4, since the scanning signal Gn serves as a low level and TFT50 is turned off, an electric charge does not flow into the sub pixel Ps via the data line 3. On the other hand in the applicable time limit T4, signal Gmon1 becomes high-level, and TFT60 is turned on. Since signal Gn-1 and signal Gn-2 become high-level, TFT51 and TFT54 will be in an ON state. Therefore, if it is in a read-out period, the voltage of the binary read from the memory Ma is written in the sub pixel Ps (m, n1) and the sub pixel Ps (m, n2), and the voltage of the binary read from the memory Mb is written in the sub pixel Ps (m+1, n1) and the sub pixel Ps (m+1, n2). Since TFT65 is an ON state at this time, by the inverters 63 and 64, a loop is formed and the voltage of the capacity 62 is held.

0055

If it is in the period T5 shown in drawing 11, TFT60 will be in an OFF state and TFT61 will be in an ON state. For this reason, if the voltage level of the capacity 62 is high-level, the voltage of a low level will be written in in the course of the inverter 63 ->TFT61 -> sub pixel Ps. It enables this to reverse the voltage impressed to a liquid crystal with a given period.

0056

Thus, according to liquid crystal panel AA concerning this embodiment, while the gradation according to number-of-bits N of inputted-image-data D can be displayed on each sub pixel in the 1st mode, in the 2nd mode, a picture can be displayed by an area gradient method according to the number of bits of the memory Ma. And power consumption can be substantially reduced by changing the 1st mode and the 2nd mode to a display image according to ** ******, without degrading the imaging quality seen from the user. According to this liquid crystal panel AA, since one memory was made to serve a double purpose by two or more sub pixels, the occupation area of a memory is decreased and a numerical aperture improves. As a result, liquid crystal panel AA becomes possible **displaying a bright picture moreover with low power consumption** . Since composition was made simple, a defective fraction can be lowered.

0057

<Mechanical constitution of 1-6:liquid crystal panel AA>

Drawing 13 is a perspective view showing the composition of liquid crystal panel AA, and drawing 14 is a sectional view of the Z-Z' line in drawing 13. As shown in these figures, liquid crystal panel AA, The element substrates 151, such as glass with which the picture element electrode 6 grade was formed, and the transparent counter substrates 152, such as glass with which the common electrode 158 grade was formed, A fixed gap is maintained by the sealant 154 in which the spacer 153 was mixed, and while pasting together so that an electrode formation face may counter mutually, it has structure which enclosed the liquid crystal 155 as electrooptic material with this gap. Although the sealant 154 is formed along the substrate circumference of the counter substrate 152, in order to enclose the liquid crystal 155, the part is carrying out the opening of it. For this reason, that opening part is closed with the sealing agent 156 after enclosure of the liquid crystal 155.

0058

Here, it is an opposed face of the element substrate 151, and in one side of outsides of the sealant 154, the data line driving circuit 200 is formed and it has the composition of driving the data line 3 which extends in the direction of Y. Two or more bonding electrodes 157 are formed in this one side, and it has the composition of inputting the various signals and picture signal from the timing generating circuit which is not illustrated. The scanning line driving circuit 100A is formed in one side which adjoins this one side, and it has at it the composition of driving the scanning line 2 which extends in the direction of X from both sides, respectively.

0059

On the other hand, electrical continuity with the element substrate 151 is planned by the conduction material in which the common electrode 158 of the counter substrate 152 was formed at at least one place among four corners in a pasting portion with the element substrate 151. Otherwise to the counter substrate 152, according to the use of liquid crystal panel AA. For example, the light filter arranged **1st** stripe shape, mosaic shape, the shape of a triangle, etc. is provided, Black matrices, such as resin black which distributed metallic materials, such as chromium and nickel, carbon, titanium, etc. to photoresist, are provided in the 2nd, for example, and the back light which irradiates the 3rd at liquid crystal panel AA is provided. A black matrix is provided in the counter substrate 152, without forming a light filter in particular in the case of the use of colored light abnormal conditions. The light-shielding film which shades light is formed in the adjacent spaces of the counter substrate 152, and the frame which is non display regions by this is formed.

0060

It adds, and while an orienting film etc. by which rubbing treatment was carried out in the predetermined direction, respectively are provided in an opposed face of the element substrate 151 and the counter substrate 152, a polarizing plate (graphic display abbreviation) according to an orientation direction is provided in each that back side, respectively. However, since efficiency for light utilization will increase as a result of the above-mentioned orienting film, a polarizing plate, etc. becoming unnecessary if a polymer dispersed liquid crystal distributed as a minute grain is used into a polymer as the liquid crystal 155, in points, such as a rise in luminosity and low power consumption, it is advantageous.

0061

Some or all of a peripheral circuit, such as the data line driving circuit 200 and the scanning line driving circuit 100A, Instead of forming in the element substrate 151, an IC chip for a drive which used TAB (Tape AutomatedBonding) technology and was mounted in a film, for example, It is good also as composition connected electrically and mechanically via an anisotropy electric conduction film provided in a specified position of the element substrate 151, and, It is good also as composition which connects the IC chip for a drive itself to a specified position of the element substrate 151 electrically and mechanically via an anisotropy electric conduction film using COG (Chip On Grass) technology.

0062

<2. a 2nd embodiment>
A liquid crystal device concerning a 2nd embodiment is constituted like a liquid crystal device of a 1st embodiment except for a point that the main pixel P is provided with the three sub pixels Ps, and a point of using the scanning line driving circuit 100B instead of the scanning line driving circuit 100A.

0063

Drawing 15 is a key map showing the pixel configuration of a 2nd embodiment. As shown in this figure, the main pixel P is carrying out form of L shape, and is provided with the three sub pixels Ps. And it has two memories per pixel. The data for controlling the gradation of the one sub pixel Ps in one memory is memorized, and the data for controlling the gradation of the two sub pixels Ps in the memory of another side is memorized.

0064

Drawing 16 is a circuit diagram showing the composition of a pixel. The main pixel P1 contains the sub pixel Ps (m, n), Ps (m+1, n), and Ps (m+1, n+1), and the main pixel P2 contains the sub pixel Ps (m, n+1), Ps (m, n+2), and Ps (m+1, n+2). In this example, while the signal Gmrw (n) controls writing and read-out of the data to the memory Man and the memory Mbn which are contained in the main pixel P1, the signal Gmrw (n+1) controls writing and read-out of the data of memory Man+1 and memory Mbn+1. Signal Gc1 controls the writing of signal Sm **to the main pixel P1** , and Sm+1, and signal Gc2 controls the writing of signal Sm **to the main pixel P2** , and Sm+1.

0065

If its attention is paid to the main pixel P1, while memorizing 1-bit data respectively to the memory Man and Man+1 and controlling the gradation of the sub pixel Ps (m, n) by this example in the 2nd mode according to the memory content of the memory Man, According to the memory content of the memory Mbn, the gradation of the sub pixel Ps (m+1, n) and the sub pixel Ps (m+1, n+1) is controlled. By this, the main pixel P1 becomes possible **displaying the gradient according to the number of the sub pixels Ps used as one** . If the data specifically memorized by Da and the memory Mbn in the data memorized by the memory Man is set to Db, and white shall be displayed for black at the time of 0 when said data is 1, The three sub pixels Ps are black, Da=0, and Db=1 in Da=Db=1, and, in the one sub pixel Ps, the three sub pixels Ps serve as **the two sub pixels Ps** white by black, Da=1, and Db=0 black, Da=0, and Db=0. Therefore, the display of 4 gradation is attained using the three sub pixels Ps. That is, according to this pixel configuration, as compared with a 1st embodiment, it becomes possible to make the gradation number per **in the 2nd mode** sub pixel Ps increase.

0066

The timing chart which drawing 17 is a circuit diagram showing the composition of the scanning line driving circuit 100B, and shows operation of a liquid crystal device **in / in drawing 18 / the 1st mode** , The timing chart and drawing 20 in which operation of a liquid crystal device **in / in drawing 19 / the write period in the 2nd mode** is shown are a timing chart which shows operation of the liquid crystal device in the read-out period in the 2nd mode. In drawing 17 - drawing 20, it explains here by the case where the representative circuit schematic of drawing 16 is set to n= 1.

0067

If the scanning line 2 is chosen one by one in order of signal Gc1, Gc2, and -- in the 1st mode and the signal G1, G2, and -- become active one by one, in the period t1, a signal level (the "1st line signal" in drawing 18) will be written in the sub pixels Ps (m, 1) and Ps (m+1, 1). In the period t2 following this, a signal level (the "2nd line signal" in drawing 18) is written in the sub pixels Ps (m, 2) and Ps (m+1, 2), and a signal level (the "3rd line signal" in drawing 18) is further written in the sub pixels Ps (m, 3) and Ps (m+1, 3) in the period t3. In the 1st mode, the signal Gmon (1, 1), the signal Gmon (1, 2), and the signals Gmon (1, 3) and Gmon (1, 4) serve as a low level, and each memory and each sub pixel Ps are separated.

0068

Next, in the write period in the 2nd mode, since signal Gmon2 is set to a low level while signal Gmon1 becomes high-level, as shown in drawing 19, TFT60 will be in an ON state and TFT61 will be in an OFF state. And in the period t2, t3, and --, signal Gmrw1,

Gmrw2, and -- become active one by one. Therefore, the data impressed to Sm and Sm+1 in the period t2 is written in memory Ma1 and Mb1, respectively, and the data impressed to Sm and Sm+1 in the period t3 is written in memory Ma2 and Mb2, respectively.

0069

Next, in the read-out period in the 2nd mode, the Y clock signal CKY is not supplied but the scanning line driving circuit 100B suspends operation. For this reason, signal Gc1, Gc2, and -- are set to a low level, and the signal G1, G2, and -- become high-level. On the other hand, signal Gmon1 and signal Gmon2 are reversed with the 1 field period 1V. While the voltage of the capacity 62 is written in each sub pixel Ps since signal Gmon1 becomes active if it is in the period T4, since signal Gmon2 becomes active in the period T5, the voltage which reversed the voltage of the capacity 62 is written in each sub pixel Ps. It becomes possible to reverse the voltage impressed to a liquid crystal by this.

0070

According to liquid crystal panel AA of a 2nd embodiment, power consumption can be substantially reduced by **which both change the 1st mode and the 2nd mode to a display image according to** ** ****** the ability to make the number of gradients increase in the 2nd mode, without degrading imaging quality seen from a user.

0071

<3. application>

<3-1: >, such as composition of an element substrate

In each embodiment mentioned above, a field which carries the memories Ma and Mb in a part of picture element region A, and a field which allocated only the sub pixel Ps may be provided. especially -- the 2nd mode -- low -- what is necessary is just to arrange the main pixel P into a portion for which a minute display is sufficient

While transparent insulating substrates, such as glass, constitute the element substrate 151 of liquid crystal panel AA and forming a silicon thin film on the substrate concerned in each embodiment mentioned above, Although TFT by which a source, a drain, and a channel were formed on the thin film concerned explained as what constitutes an element of a switching element of a pixel, the data line driving circuit 200, and the scanning line driving circuits 100A and 100B, this invention is not restricted to this. This invention is applicable to a liquid crystal panel in which all the peripheral circuits required for a drive of a liquid crystal panel were formed on an element substrate, using TFT. This invention is applicable not only to said peripheral circuit but a liquid crystal panel in which a microprocessor, a memory, an interface circuit, a converter, a timing generator, an image processing circuit, etc. were formed on an element substrate. such technology is called "system one glass (System on glass)" or "system LCD."

0072

For example, a semiconductor substrate may constitute the element substrate 151 and the insulated gate field effect transistor by which the source, the drain, and the channel were formed in the surface of the semiconductor substrate concerned may constitute the switching element of a pixel, and the element of various kinds of circuits. Thus, since it cannot use as a transmission type display panel when a semiconductor substrate constitutes the element substrate 151, the picture element electrode 6 will be formed with aluminum etc., and it will be used as a reflection type. The picture element electrode 6 may only be used as a reflection type by using the element substrate 151 as a transparent base.

0073

If it was in the embodiment mentioned above, the switching element of the pixel was explained as 3 terminal elements represented with TFT, but it may constitute from 2 terminal elements, such as a diode. However, in using 2 terminal elements as a switching element of a pixel, while forming the scanning line 2 in one substrate and forming the data line 3 in the substrate of the other, it is necessary to form 2 terminal elements between either one of the scanning line 2 or the data line 3 and a picture element electrode. In this case, a pixel will comprise a one terminal pair network element by which the series connection was carried out between the scanning line 2 and the data line 3, and a liquid crystal.

0074

Although this invention was explained as an active matrix type liquid crystal display device, it is not restricted to this but can be applied also to the PASSHIIBU type using a STN (Super Twisted Nematic) liquid crystal etc. As electrooptic material, an organic light emitting diode (OLED) element or an electroluminescence (EL) element other than a liquid crystal, etc. can be used, and it can apply also to the display device which displays according to the electrooptic effect.

0075

Composition of a pixel of an electrooptics panel which used an organic light emitting diode element is shown in drawing 21 as an example. It is the following points that main pixel P' shown in drawing 21 is different from the main pixel P shown in drawing 2. A point of having formed the current supply source line 80 for supplying current to the OLED elements 73 and 75 in the 1st, It is the point of 2nd having lost a point of having formed TFT72 of a P channel, 74, and the OLED elements 73 and 75 instead of the storage capacitance 52 and 55 and the liquid crystal capacity 53 and 56, and a system controlled by Gmon2 by the 3rd. If those gate voltage is set to a low level, TFT72 and 74 will be in an ON state, and will supply current to the OLED elements 73 and 75 from the current supply source line 80. Thereby, while one, the sub pixel Ps turns off the sub pixel Ps, if TFT72 and 74 are turned off. By this, gradation will be controlled in binary. Since an OLED element is driven by DC, the number of ** without the necessity of carrying out polarity reversals unlike a case where a liquid crystal is driven, and the signals Gmon which control connection between a memory and a sub circuit for this reason is one sufficient.

0076

The embodiment mentioned above is applicable to a plasma display etc. That is, this invention is applicable to the liquid crystal device mentioned above and all the electro-optic devices which have similar composition.

0077

<3-2: Electronic device >

<3-2-1:mobile type computer>

Next, the example which applied this liquid crystal panel AA to the mobile type personal computer is explained. Drawing 22 is a perspective view showing the composition of this personal computer. In the figure, the computer 1200 comprises the body part 1204 provided with the keyboard 1202, and the liquid crystal display unit 1206. This liquid crystal display unit 1206 is constituted by adding a back light to the back of the liquid crystal panel 1005 described previously.

0078

<3-2-3: Cellular-phone >

The example which applied this liquid crystal panel AA to the cellular phone is explained. Drawing 23 is a perspective view showing the composition of this cellular phone. In a figure, the cellular phone 1300 is provided with the reflection type liquid crystal panel 1005 with two or more manual operation buttons 1302. If it is in this reflection type liquid crystal panel 1005, a front light is provided in that front face if needed.

0079

Besides an electronic device explained with reference to drawing 22 and drawing 23, a liquid crystal television, ****** provided with a video tape recorder of a view finder type and a monitor direct viewing type, a car navigation device, pager, an electronic notebook, a calculator, a word processor, a workstation, a TV phone, a POS terminal, and a touch panel etc. are mentioned. And it cannot be overemphasized that can apply to these various electronic equipment.

Brief Description of the Drawings

Drawing 1 It is a block diagram showing the entire configuration of the liquid crystal device concerning a 1st embodiment of this invention.

Drawing 2 It is a circuit diagram showing the detailed composition of the main pixel P formed in the equipment corresponding to intersection with scanning line 2-n1 - 2-n6, data-line 3-m, and 3-m+1.

Drawing 3 It is a key map for explaining the relation between the main pixel P in the equipment, and the sub pixel Ps.

Drawing 4 It is a block diagram showing the composition of the scanning line driving

circuit 100A of the equipment.
Drawing 5 It is a circuit diagram showing the composition of unit shift circuit Ua2n-1 of the scanning line driving circuit 100A of the equipment - Ua2n+1, and Logical unit Ubn.
Drawing 6 It is a circuit diagram showing the composition of the data line driving circuit 200 of the equipment.
Drawing 7 It is a timing chart of the various signals in the 1st mode of the equipment.
Drawing 8 It is a key map showing the flow of the signal of the write period in the 1st mode of the equipment.
Drawing 9 It is a timing chart which shows operation of the write period in the 2nd mode of the equipment.
Drawing 10 It is a key map showing the flow of the signal of the write period in the 2nd mode of the equipment.
Drawing 11 It is a timing chart which shows operation of the read-out period in the 2nd mode of the equipment.
Drawing 12 It is a key map showing the flow of the signal of the read-out period in the 2nd mode of the equipment.
Drawing 13 It is a perspective view explaining the composition of liquid crystal panel AA of the equipment.
Drawing 14 It is a partial sectional view for explaining the structure of liquid crystal panel AA of the equipment.
Drawing 15 It is a key map showing the pixel configuration of the liquid crystal device concerning a 2nd embodiment.
Drawing 16 It is a circuit diagram showing the detailed composition of the pixel of the equipment.
Drawing 17 It is a circuit diagram showing the composition of the scanning line driving circuit 100B of the equipment.
Drawing 18 It is a timing chart which shows the operation in the 1st mode of the equipment.
Drawing 19 It is a timing chart which shows operation of the write period in the 2nd mode of the equipment.
Drawing 20 It is a timing chart which shows the operation in the read-out period in the 2nd mode of the equipment.
Drawing 21 It is a circuit diagram showing an example of the pixel configuration of the electrooptics panel using an OLED element.
Drawing 22 It is a perspective view showing the composition of an example slack personal computer of the electronic device which applied liquid crystal panel AA.
Drawing 23 It is a perspective view showing the composition of an example slack cellular phone of the electronic device which applied liquid crystal panel AA.
Explanations of letters or numerals
AA **-- The data line, 6 / -- Picture element electrode,** -- A liquid crystal panel, A -- A picture element region, 2 -- A scanning line, 3 50 -- TFT (switching element), 100A, 100B -- Scanning line driving circuit, 200 .... A data line driving circuit, Ps -- The sub pixel Ps, P -- Main pixel, 50 **-- Capacity, 63, 64 / -- An inverter (the 1st and 2nd inverting circuit), 65 / -- TFT (the 4th switching element).** -- TFT (the 1st switching element), 60 -- TFT (the 2nd switching element), 61 -- TFT (the 3rd switching element), 62

Field of the Invention
This invention relates to the electrooptics panel etc. which equipped the pixel with the memory function.
0002

Description of the Prior Art
The liquid crystal panel of an active matrix is provided with the following.

The element substrate by which the switching element was mainly provided in each of the picture element electrode arranged to matrix form.
The counter substrate in which the light filter etc. were formed.
The liquid crystal with which it filled up among these both boards.
In such composition, if a scanning signal is impressed to a switching element via a scanning line, the switching element concerned will be in switch-on. If a picture signal is impressed to a picture element electrode via the data line in the case of this switch-on, a predetermined electric charge will be accumulated in the liquid crystal layer between the picture element electrode concerned and a counterelectrode (common electrode).

0003

In such a liquid crystal panel, the light transmittance of a liquid crystal changes according to impressed electromotive force. By changing the voltage written in liquid crystal capacity, the voltage gradient method on which gradation is displayed is well-known. On the other hand, one pixel is divided into two or more sub pixels, and the area gradation method for realizing a gradation display by giving an on-off indication of these sub pixels is known (for example, patent documents 1).

0004

The liquid crystal device provided with the mode in which the gradation display by an area gradation method is performed according to the data which provided one memory in one sub pixel, and was memorized, and the mode in which a gradation display is performed by a voltage gradation method is also known (for example, patent documents 2).

0005

Patent documents 1

JP,2001-281628,A (drawing 2 and drawing 3)

0006

Patent documents 2

JP,2002-22957,A (Claim 1 and drawing 4)

0007

Problem to be solved by the invention

By the way, it is needed that the occupation area of a memory is small for the luminosity of an electrooptics panel being influenced by the numerical aperture and raising a numerical aperture. However, since one memory was arranged at one sub pixel if it was in the conventional electrooptics panel, there was a problem that a display image became dark.

0008

This invention is made in view of a situation mentioned above, and makes it solution SUBJECT to provide an electrooptics panel which decreased an occupation area of a memory etc.

0009

Means for solving problem

In order to solve an aforementioned problem, a drive method of an electrooptics panel concerning this invention, Have a sub pixel provided corresponding to intersection of a scanning line, two or more data lines, and two or more said scanning lines and said data lines, and a main pixel which has said two or more sub pixels, and said main pixel, It has one or more memories which memorize image data of M (M is natural number) bit, The number of said sub pixels matched with per said memory is 1 how to drive an electrooptics panel which exceeds, and in the 1st mode. Based on image data of N (N>=M and N are natural numbers) bit, display gradation of N bit on said each sub pixel, and in the 2nd mode. While memorizing image data of M bit in said each memory, gradation of M bit is displayed on said sub pixel matched with said each memory.

0010

According to this invention, in the 1st mode, a high definition picture can be displayed and a picture with low resolution and gradation number can be displayed in the 2nd mode as compared with the 1st mode. When displaying Still Picture Sub-Division, it becomes unnecessary to rewrite a memory content of a memory, since the 2nd mode serves as a display which used a memory function. Therefore, since a scanning line and the data line are chosen one by one and it becomes unnecessary to drive them, it becomes possible to reduce power consumption substantially.

0011

In said 1st mode, write here the signal generated based on the image data of N bit in said each sub pixel, and in said 2nd mode. It is preferred to display the gradation of M bit in common with said sub pixel connected to the memory concerned based on the image data which memorized the image data of M bit in said memory, and was read from said memory. In this case, in the 2nd mode, although the sub pixel connected to a certain memory will display the gradation of M bit, since the main pixel can have two or more memories, the gradation display of it by an area gradation method is attained.

0012

Said M bit is 1 bit and it is preferred to display the gradation of each of said sub pixel in binary in said 2nd mode. According to this invention, structure of a memory is made simple and it becomes possible to perform image display in the 2nd mode by easy control.

0013

It adds, and it is possible to output selectively data and the inversion data which reversed this, and, as for said memory, it is desirable to read said data and said inversion data from said memory with a given period, and to supply said sub pixel. To use a liquid crystal as electrooptic material, it is necessary to carry out the alternating current drive of the liquid crystal from the viewpoint which prevents a printing phenomenon. According to this invention, in the 2nd mode, since it becomes possible to reverse the voltage read from a memory focusing on reference level, the alternating current drive of the liquid crystal can be carried out.

0014

An electrooptics panel concerning this invention Next, two or more scanning lines and two or more data lines, Have a sub pixel provided corresponding to intersection of said scanning line and said data line, and a main pixel which has said two or more sub pixels, and said main pixel, It has one or more memories which memorize image data of M (M is natural number) bit, and the number of said sub pixels matched with per said memory exceeds 1. According to this invention, since the number of said sub pixels matched with per memory exceeds 1, area of a memory occupied to a viewing area is reducible. Since a memory area does not contribute to a penetration of light, it can raise a numerical aperture by reducing occupation areas. As a result, it is bright and, moreover, an electrooptics panel with little power consumption can be provided. If a certain memory is matched with one sub pixel, other memories are matched with two sub pixels, and are and it concludes as a whole that the number of sub pixels matched with per memory exceeds 1, a case where it is matched with one or more memories is included.

0015

Here, said data line and one input/output terminal are connected, an input/output terminal of another side is provided with the 1st switching element connected with wiring, and, as for said main pixel, it is **said wiring** preferred to connect said one or more sub pixels corresponding to said memory. This 1st switching element may be provided for every data line, and the 1st two or more switching element may be contained in one main pixel.

0016

As for said main pixel, it is preferred to have the switching means established between said memory and said wiring. By this switching means, a memory is separated and connected with a sub pixel.

0017

Said switching means is provided with the 2nd switching element and the 3rd switching element, and more specifically said memory, The 1st inverting circuit where the capacity to which said 2nd switching element and one terminal are connected, and one terminal

and input terminal of said capacity are connected, It is preferred to have the 2nd inverting circuit where an input terminal is connected to said 3rd switching element and the output terminal of said 1st inverting circuit, and the 4th switching element provided between the output terminal of said 2nd inverting circuit and one terminal of said capacity.

0018

A main pixel may consist of said a part of two or more of said sub pixels. That is, only the portion (main picture element part) by which the 1st mode and the 2nd mode are applied into a viewing area, and the 1st mode are applied, and may carry out partial mixture. Although the screen which awaits a telephone call is displayed in a cellular phone, such a screen has a portion which displays an icon etc. on the upper part or the lower part. Then, low power consumption is realizable by arranging a main pixel into such a portion.

0019

Next, the scanning line driving circuit concerning this invention drives the electrooptics panel mentioned above, and in the 1st mode. In **make said 1st switching element of said main pixel into an ON state one by one via a scanning line, and** the "on" period concerned, In **choose said sub pixel contained in the main pixel concerned one by one along said scanning line, and** the write period in the 2nd mode, Said 1st switching element is made into an ON state one by one via said scanning line, In **in the "on" period concerned, control said 2nd switching element via said scanning line to make an ON state and said 3rd switching element into an OFF state, and to make said 4th switching element into an OFF state, and** the read-out period in the 2nd mode, It controls via said scanning line to turn an OFF state on and off for said 1st switching element, and to make an ON state, said 2nd switching element, and said 3rd switching element turn said 4th switching element on and off exclusively with a given period.

0020

According to this invention, in the 1st mode, each sub pixel can be chosen one by one, data is written in a memory and the write period in the 2nd mode enables it to read data and inversion data from a memory by turns, and to supply each sub pixel in the read-out period in the 2nd mode.

0021

Next, the data line driving circuit concerning this invention is used for the electrooptics panel mentioned above, Have a means to generate the sampling pulse which shifts a start pulse according to a clock signal, and becomes active exclusive one by one, and in the 1st mode. While sampling respectively the picture signal which obtained the image data of said N bit by changing it into an analog signal based on said sampling pulse and supplying said data line one by one, In the write period in said 2nd mode, the image data of said M bit is respectively sampled based on said sampling pulse, said data line is supplied one by one, and if it is in the read-out period in the 2nd mode, operation is suspended. when a high definition display is required according to this data line driving circuit, while supplying the picture signal which can display the gradation of N bit to the data line -- low -- when a minute display is sufficient, since a read-out period suspends operation, it can reduce power consumption substantially by only the write period operating.

0022

Next, the electronic device concerning this invention is provided with the electrooptics panel mentioned above. For example, a view finder, a portable telephone, a notebook computer, a video projector, etc. which are used for a liquid crystal device and a video camera correspond.

0023

Mode for carrying out the invention

Hereafter, the embodiment of this invention is described with reference to Drawings.

<1. a 1st embodiment>

<1-1: Entire configuration **of a liquid crystal device** >

First, the electro-optic device concerning the embodiment of this invention is explained. This electro-optic device is a transmission type liquid crystal device which performs a predetermined display by that electrooptic change using a liquid crystal as electrooptic

material. The main pixel P is constituted from the four sub pixels Ps by this liquid crystal device. And in the 1st mode, while writing the voltage according to gradation in each sub pixel Ps and displaying a picture, in the 2nd mode, each sub pixel Ps is driven with a binary, and image display by an area gradation method is performed.

0024

Drawing 1 is a block diagram showing the entire configuration of the liquid crystal device concerning an embodiment. This liquid crystal device is provided with liquid crystal panel AA and the timing generating circuit 300. Liquid crystal panel AA is provided with the picture element region A, the scanning line driving circuit 100A, and the data line driving circuit 200 on the element substrate.

0025

Inputted-image-data D supplied to this liquid crystal device is the form of three bit parallels, for example. Synchronizing with inputted-image-data D, the timing generating circuit 300 The Y clock signal CKY, Reversal Y clock signal CKYB, X clock signal CKX, reversal X clock signal CKXB, the Y transfer starting pulse SPY, and X transfer starting pulse SPX are generated, and the scanning line driving circuit 100A and the data line driving circuit 200 are supplied.

0026

Here, the Y clock signal CKY specifies the period which chooses the scanning line 2, and reversal Y clock signal CKYB reverses the logical level of the Y clock signal CKY. X clock signal CKX specifies the period which chooses the data line 3, and reversal X clock signal CKXB reverses the logical level of X clock signal CKX.

0027

Next, as shown in drawing 1, while the scanning line 2 of a lot arranges in parallel and is formed in accordance with the direction of J group X by six, in accordance with the direction of Y, the data line 3 of K (K is two or more natural numbers) book arranges in the picture element region A in parallel, and is formed in it. And the sub pixel Ps is formed in near intersection of the scanning line 2 and the data line 3. Since the sub pixel Ps is specified **the following explanation** , when the number of Y ("Y" as shown a scanning line in drawing 1, when it expresses with 2-YV), and the data line is set to X ("X" as shown the data line in drawing 1, when it expresses with 3-X) for the group number item of a scanning line, The sub pixel corresponding to scanning line 2-Y2 shall be expressed with Ps (X, Y1), and the sub pixel corresponding to scanning line 2-Y3 shall be expressed with Ps (X, Y2).

0028

<1-2: Pixel configuration >

Drawing 2 is a circuit diagram showing the detailed composition of the main pixel P formed corresponding to intersection with scanning line 2-n1 - 2-n6, data-line 3-m, and 3-m+1. As shown in this figure, the main pixel P is provided with the four sub pixels Ps (m, n1), Ps (m, n2), Ps (m+1, n1) and Ps (m+1, n2), TFT50, TFT60, TFT61 and the memory Ma, and Mb.

0029

The sub pixel Ps (m, n1) has TFT51, the storage capacitance 52, and the liquid crystal capacity 53. The liquid crystal capacity 53 is constituted by a picture element electrode, a counterelectrode, and the liquid crystal with which it fills up among them. Other sub pixels Ps as well as the sub pixel Ps (m, n1) are constituted.

0030

A gate is connected to scanning line 2-n1, a source is connected to data-line 3-m, and, as for TFT50 of an upper left end, a drain is further connected to the sub pixels Ps (m, n1) and Ps (m, n2). In the write period of the image data in the write period of a picture signal in the 1st mode, and the 2nd mode, TFT50 will be in an ON state, and will be in an OFF state in a display period. TFT50 is controlled by the scanning signal Gn supplied by scanning line 2-n1.

0031

TFT60 and 61 are used in order to control whether the sub pixels Ps (m, n1) and Ps (m, n2) are connected with the memory Ma. A gate of TFT60 is connected to scanning line 2-n4, the source is connected with a drain of TFT50, and the drain is further connected with the memory Ma. A gate of TFT61 is connected to scanning line 2-n5, the source is

connected with a drain of TFT50, and the drain is further connected with the memory Ma. Turning on and off of TFT60 is controlled by signal Gmon1, and turning on and off of TFT61 is controlled by signal Gmon2.

0032

The memory Ma is provided with the capacity 62, the inverters 63 and 64, and TFT65. If one **TFT65** , latch circuitry will be formed by the inverters 63 and 64. Therefore, voltage of the capacity 62 will be held. On the other hand, since a loop is not formed if TFT65 turns off, it becomes possible to write voltage in the capacity 62. Therefore, if TFT65 is made one after writing voltage in the capacity 62, voltage written in the capacity 62 can be held. That is, the memory Ma functions as one bit memory. Turning on and off of TFT65 is controlled by the signal Gmrwn supplied via scanning line 2-n6. The signal Gmrwn points to writing of data with a low level, is high-level and directs read-out (maintenance) of data.

0033

While memorizing 1-bit data respectively in the memories Ma and Mb and controlling gradation of the sub pixel Ps (m, n1) and the sub pixel Ps (m, n2) by this example in the 2nd mode according to a memory content of the memory Ma, According to a memory content of the memory Mb, gradation of the sub pixel Ps (m+1, n1) and the sub pixel Ps (m+1, n2) is controlled. By this, the main pixel P becomes possible **displaying a gradient according to the number of the sub pixels Ps used as one** . If data specifically memorized by Da and the memory Mb in data memorized by the memory Ma is set to Db, and white shall be displayed for black at the time of 0 when said data is 1, By Da=Db=1, in black and remaining two sub pixels, the four sub pixels Ps serve as **the two sub pixels Ps** white by black, Da=1, Db=0 or Da=0, and Db=1 white and Da=Db=0, and a display of 3 gradation of the four sub pixels Ps is attained.

0034

Although 1-bit data was memorized to the memory Ma and Mb, it may be made to memorize data of M bit in a memory in an example shown in drawing 2, as shown in drawing 3 (A). Here, if the number of bits of inputted-image-data D is set to N, it will become N>=M (N and M are natural numbers). That is, in the 1st mode, N fatbits uses each sub pixel Ps (gradation is displayed 2^N), and M fatbits makes it a sub pixel (this example two pieces) connected with one memory in the 2nd mode. Although the main pixel P in drawing 3 (A) contained the four sub pixels Ps, the main pixel P which contains the two sub pixels Ps as shown in drawing 3 (B) may be assumed.

0035

Although resolution and a display gradient deteriorate as compared with the 1st mode, since a display in the 2nd mode has memorized gradation to the memory Ma and Mb, it does not need to scan each sub pixel Ps and does not need to write in a picture signal. Therefore, since it becomes unnecessary to operate the scanning line driving circuit 100A and the data line driving circuit 200 synchronizing with a clock signal, it becomes possible to reduce power consumption substantially. In particular, in portable electronic devices, such as a portable telephone and PDA, there is a period which shows a menu screen provided with two or more icons. As compared with a case where video is displayed, low performance is sufficient for resolution and a display gradient required in order to display such a menu screen. Therefore, it becomes possible to long-time-ize time to operate with a battery, without spoiling imaging quality seen from a user by displaying a menu screen etc. in the 2nd mode.

0036

<1-3: Composition **of a scanning line driving circuit** >

Drawing 4 is a block diagram showing composition of the scanning line driving circuit 100A, and drawing 5 is a circuit diagram showing composition of unit shift circuit Ua2n-1 of the scanning line driving circuit 100A - Ua2n+1, and Logical unit Ubn. As shown in these figures, the scanning line driving circuit 100A is provided with the shift register 110, the logic circuit group 120, and the inverter 130.

0037

The shift register 110 is provided with unit shift circuit Ua1 **2J+1 piece** - Ua2J+1, shifts the Y transfer starting pulse SPY one by one synchronizing with the Y clock signal CKY and reversal Y clock signal CKYB, and outputs a shift signal respectively. Unit shift circuit

Ua1 - Ua2J+1 are provided with the clocked inverters 111 and 112 and the inverter 113. In unit shift circuit Ua2n-1, the Y clock signal CKY becomes high-level and active, and the clocked inverter 111 becomes high-level **inversion clock signal CKYB** and active **the clocked inverter 112** . If the Y clock signal CKY is in the period of high level, the Y transfer starting pulse SPY is outputted as a shift signal via the clocked inverter 111 and the inverter 113. On the other hand, latch circuitry is formed by the clocked inverter 112 and the inverter 113 in the period when inversion clock signal CKYB is high-level. Therefore, the logical level of a shift signal is held an applicable time limit. As a result, as for the shift signal outputted from a unit shift circuit, the active period length of adjacent signals becomes that with which only the half cycle of the Y clock signal CKY lapped.

0038

The logic circuit group 120 is provided with J Logical unit Ub1-UbJ. Each Logical unit Ub1-UbJ supports the three unit shift registers Ua. n-th Logical unit Ubn corresponds to 2n - the 1st unit-shift-registers Ua2n-1 and 2n position unit-shift-registers Ua2n, and unit-shift-registers Ua2n+1 **2n+1 position** . Each Logical unit Ub1-UbJ is respectively provided with NAND circuits 121-125.

0039

<1-4: Composition **of a data line driving circuit** >

Drawing 6 is a circuit diagram showing composition of the data line driving circuit 200. As shown in this figure, the data line driving circuit 200 is provided with the shift register 210, the selection-circuitry group 220, DA converter 230, the digital buffer 240, the switches 231, 232, 241, and 242, and the signal wire 250.

0040

The shift register 210 is provided with K+1 unit shift circuit Uc1 - UcK+1, shifts X transfer starting pulse SPX one by one synchronizing with X clock signal CKX and reversal X clock signal CKXB, and outputs shift signal Gc1 - GcK+1 respectively. Unit shift circuit Uc1 - UcK+1 are provided with the clocked inverters 211 and 212 and the inverter 213. Since this composition is the same as that of the shift register 110 of the data line driving circuit 100, explanation is omitted.

0041

The selection-circuitry group 220 is provided with the K selection units Ud1-UdK. Each selection units Ud1-UdK are provided with NAND circuit 221, the inverter 222, and the sampling switch 223. A signal with which active period length lapped only a half cycle of X clock signal CKX is supplied to NAND circuit 221 from each unit shift circuit Uc1-UcK+1. Therefore, active period length is a half cycle of X clock signal CKX, and the sampling signals SP1-SPK become active exclusively.

0042

While the signal Gmem becomes high-level in a write period in the 2nd mode, it is set to a low level in a read-out period in the 1st mode and the 2nd mode. In a period of a low level, the switches 241 and 242 will be in an OFF state, while the signal Gmem will be in an ON state in a high-level period. The switches 231 and 232 are constituted so that turning on and off may change as exclusively as the switches 241 and 242.

0043

Therefore, when the signal Gmem directs a write period in the 2nd mode, as shown in a figure, the switches 241 and 242 will be in an ON state, and image data D is supplied to the signal wire 250 via the digital buffer 240. On the other hand, when the signal Gmem directs the 1st mode, a picture signal is supplied to the signal wire 250 via DA converter 230.

0044

<1-5: Operation **of a liquid crystal device** >

<1-5-1: 1st mode >

There are the 1st mode in which a display by a picture signal is performed, and the 2nd mode in which a display by image data is performed in an operating state of a liquid crystal device. A timing chart of various signals in the 1st mode is shown in drawing 7. The memories Ma and Mb are not used in the 1st mode. For this reason, the signals Gmon1 and Gmon2 serve as a low level, and the sub pixel Ps and the memories Ma and Mb which are shown in drawing 2 are separated.

0045

Only a half cycle of the Y clock signal CKY is delayed, and the signal C1 is outputted by the unit shift circuit U2n as the signal C2. NAND circuit 121 reverses and outputs a logical product with signal C2B which reversed the signal C1 and the signal C2. For this reason, the signal C4 serves as a low level in **T2** the first half of the period T1 which becomes active **the signal C1** . NAND circuit 122 reverses and outputs a logical product of the signal C2 and the signal C3B. Therefore, the signal C5 serves as a low level by T3 during the second half of the period T1.

0046

On the other hand, NAND circuits 123 and 124 reverse and output the signals C4 and C5, when the signal Gmenb is a low level. Since the signal Gmenb becomes high-level in the 1st mode, in the period T2 and period T3, signal Gn-1 and signal Gn-2 which are outputted from NAND circuits 123 and 124 are respectively set to high level (active). Since the signal Gmem has a low level in the 1st mode, the signal Gmrwn outputted from NAND circuit 125 becomes high-level.

0047

Drawing 8 is a key map showing the course of the picture signal in period T3 shown in drawing 7. Since the scanning signal Gn and Gn-2 become active if it is in period T3, as shown in drawing 8, TFT50 and TFT54 will be in an ON state. Therefore, sampling signal Sm will be written in the sub pixel Ps (m, n2), and sampling signal Sm+1 will be written in the sub pixel Ps (m+1, n2).

0048

In the 1st mode, since the switches 231 and 232 shown in drawing 6 will be in an ON state, sampling signal Sm and Sm+1 becomes an analog signal which shows gradation. Therefore, voltage according to gradation will be impressed to storage capacitance and liquid crystal capacity. And after period T3 is completed, TFT50 and TFT54 will be in an OFF state, and voltage impressed to the storage capacitance 52 and the liquid crystal capacity 53 will be held. Thereby, image display becomes possible.

0049

<1-5-2: 2nd mode >

Next, it divides and explains during **which reads data** the read-out from a write period which writes in data to the memories Ma and Mb for operation of a liquid crystal device in the 2nd mode, and them. Drawing 9 is a timing chart which shows operation of a liquid crystal device in a write period in the 2nd mode.

0050

In a write period, since the signal Gmemb serves as a low level, signal Gn-1 and Gn-2 which are the output signals of NAND circuits 123 and 124 become always high-level. Although the signal Gmem is supplied to NAND circuit 125, since it is set to the signal Gmem being high-level in a write period, the signal Gmrwn becomes what reversed the logical product of the signal C1 and the signal C2. Therefore, the signal Gmrwn serves as a low level in period T3.

0051

Drawing 10 is a key map showing the course of the picture signal in period T3 shown in drawing 9. Since the scanning signal Gn, Gn-1, and Gn-2 become active and also signal Gmon1 becomes active if it is in period T3, as shown in drawing 10, TFT50, TFT51, TFT54, and TFT60 will be in an ON state. Therefore, signal Sm is written in the sub pixel Ps (m, n1), Ps (m, n2), and the memory Ma, and signal Sm+1 is written in the sub pixel Ps (m+1, n1), Ps (m+1, n2), and the memory Mb. Since signal Gmon2 and the signal Gmrwn serve as a low level in period T3, TFT61 and 65 will be in an OFF state. For this reason, the voltage from which a logical level differs via TFT65 is not written in the capacity 62.

0052

Drawing 11 is a timing chart which shows operation of the liquid crystal device in the read-out period in the 2nd mode. First, in the read-out period in the 2nd mode, the Y clock signal CKY serves as a low level, and the Y transfer starting pulse SPY is not supplied to the scanning line driving circuit 100A. Therefore, the shift register 110 does not operate. For this reason, the signals C1 and C2 serve as a low level, and signal C2B, C3B, C4, and C5 become high-level. Since the signal Gmemb serves as a low level, it is set to signal Gn-1 and Gn-2 being high-level.

0053
Next, since the signal Gmrwn reverses the logical product of the signal C1, C2, and Gmem, it becomes high-level. In the example shown in drawing 11, the signals Gmon1 and Gmon2 are reversed with the 1 field period 1V. This is for exchange-izing voltage impressed to a liquid crystal. An inversion cycle may be an integral multiple of 1 horizontal scanning cycle.
0054
Drawing 12 is a key map showing the course of the picture signal in the period T4 shown in drawing 11. If it is in the period T4, since the scanning signal Gn serves as a low level and TFT50 is turned off, an electric charge does not flow into the sub pixel Ps via the data line 3. On the other hand in the applicable time limit T4, signal Gmon1 becomes high-level, and TFT60 is turned on. Since signal Gn-1 and signal Gn-2 become high-level, TFT51 and TFT54 will be in an ON state. Therefore, if it is in a read-out period, the voltage of the binary read from the memory Ma is written in the sub pixel Ps (m, n1) and the sub pixel Ps (m, n2), and the voltage of the binary read from the memory Mb is written in the sub pixel Ps (m+1, n1) and the sub pixel Ps (m+1, n2). Since TFT65 is an ON state at this time, by the inverters 63 and 64, a loop is formed and the voltage of the capacity 62 is held.
0055
If it is in the period T5 shown in drawing 11, TFT60 will be in an OFF state and TFT61 will be in an ON state. For this reason, if a voltage level of the capacity 62 is high-level, voltage of a low level will be written in in a course of the inverter 63 ->TFT61 -> sub pixel Ps. It enables this to reverse voltage impressed to a liquid crystal with a given period.
0056
Thus, according to liquid crystal panel AA concerning this embodiment, while gradation according to number-of-bits N of inputted-image-data D can be displayed on each sub pixel in the 1st mode, in the 2nd mode, a picture can be displayed by an area gradient method according to the number of bits of the memory Ma. And power consumption can be substantially reduced by changing the 1st mode and the 2nd mode to a display image according to ** ******, without degrading imaging quality seen from a user. According to this liquid crystal panel AA, since one memory was made to serve a double purpose by two or more sub pixels, an occupation area of a memory is decreased and a numerical aperture improves. As a result, liquid crystal panel AA becomes possible **displaying a bright picture moreover with low power consumption** . Since composition was made simple, a defective fraction can be lowered.
0057
<Mechanical constitution of 1-6:liquid crystal panel AA>
Drawing 13 is a perspective view showing the composition of liquid crystal panel AA, and drawing 14 is a sectional view of the Z-Z' line in drawing 13. As shown in these figures, liquid crystal panel AA, The element substrates 151, such as glass with which the picture element electrode 6 grade was formed, and the transparent counter substrates 152, such as glass with which the common electrode 158 grade was formed, A fixed gap is maintained by the sealant 154 in which the spacer 153 was mixed, and while pasting together so that an electrode formation face may counter mutually, it has structure which enclosed the liquid crystal 155 as electrooptic material with this gap. Although the sealant 154 is formed along the substrate circumference of the counter substrate 152, in order to enclose the liquid crystal 155, the part is carrying out the opening of it. For this reason, that opening part is closed with the sealing agent 156 after enclosure of the liquid crystal 155.
0058
Here, it is an opposed face of the element substrate 151, and in one side of outsides of the sealant 154, the data line driving circuit 200 is formed and it has the composition of driving the data line 3 which extends in the direction of Y. Two or more bonding electrodes 157 are formed in this one side, and it has the composition of inputting the various signals and picture signal from the timing generating circuit which is not illustrated. The scanning line driving circuit 100A is formed in one side which adjoins this one side, and it has at it the composition of driving the scanning line 2 which extends in

the direction of X from both sides, respectively.

0059

On the other hand, electrical continuity with the element substrate 151 is planned by the conduction material in which the common electrode 158 of the counter substrate 152 was formed at at least one place among four corners in a pasting portion with the element substrate 151. Otherwise to the counter substrate 152, according to the use of liquid crystal panel AA. For example, the light filter arranged **1st** stripe shape, mosaic shape, the shape of a triangle, etc. is provided, Black matrices, such as resin black which distributed metallic materials, such as chromium and nickel, carbon, titanium, etc. to photoresist, are provided in the 2nd, for example, and the back light which irradiates the 3rd at liquid crystal panel AA is provided. A black matrix is provided in the counter substrate 152, without forming a light filter in particular in the case of the use of colored light abnormal conditions. The light-shielding film which shades light is formed in the adjacent spaces of the counter substrate 152, and the frame which is non display regions by this is formed.

0060

It adds, and while an orienting film etc. by which rubbing treatment was carried out in the predetermined direction, respectively are provided in an opposed face of the element substrate 151 and the counter substrate 152, a polarizing plate (graphic display abbreviation) according to an orientation direction is provided in each that back side, respectively. However, since efficiency for light utilization will increase as a result of the above-mentioned orienting film, a polarizing plate, etc. becoming unnecessary if a polymer dispersed liquid crystal distributed as a minute grain is used into a polymer as the liquid crystal 155, in points, such as a rise in luminosity and low power consumption, it is advantageous.

0061

Some or all of a peripheral circuit, such as the data line driving circuit 200 and the scanning line driving circuit 100A, Instead of forming in the element substrate 151, an IC chip for a drive which used TAB (Tape AutomatedBonding) technology and was mounted in a film, for example, It is good also as composition connected electrically and mechanically via an anisotropy electric conduction film provided in a specified position of the element substrate 151, and, It is good also as composition which connects the IC chip for a drive itself to a specified position of the element substrate 151 electrically and mechanically via an anisotropy electric conduction film using COG (Chip On Grass) technology.

0062

<2. a 2nd embodiment>

A liquid crystal device concerning a 2nd embodiment is constituted like a liquid crystal device of a 1st embodiment except for a point that the main pixel P is provided with the three sub pixels Ps, and a point of using the scanning line driving circuit 100B instead of the scanning line driving circuit 100A.

0063

Drawing 15 is a key map showing the pixel configuration of a 2nd embodiment. As shown in this figure, the main pixel P is carrying out form of L shape, and is provided with the three sub pixels Ps. And it has two memories per pixel. The data for controlling the gradation of the one sub pixel Ps in one memory is memorized, and the data for controlling the gradation of the two sub pixels Ps in the memory of another side is memorized.

0064

Drawing 16 is a circuit diagram showing the composition of a pixel. The main pixel P1 contains the sub pixel Ps (m, n), Ps (m+1, n), and Ps (m+1, n+1), and the main pixel P2 contains the sub pixel Ps (m, n+1), Ps (m, n+2), and Ps (m+1, n+2). In this example, while the signal Gmrw (n) controls writing and read-out of the data to the memory Man and the memory Mbn which are contained in the main pixel P1, the signal Gmrw (n+1) controls writing and read-out of the data of memory Man+1 and memory Mbn+1. Signal Gc1 controls the writing of signal Sm **to the main pixel P1** , and Sm+1, and signal Gc2 controls the writing of signal Sm **to the main pixel P2** , and Sm+1.

0065

If its attention is paid to the main pixel P1, while memorizing 1-bit data respectively to the memory Man and Man+1 and controlling the gradation of the sub pixel Ps (m, n) by this example in the 2nd mode according to the memory content of the memory Man, According to the memory content of the memory Mbn, the gradation of the sub pixel Ps (m+1, n) and the sub pixel Ps (m+1, n+1) is controlled. By this, the main pixel P1 becomes possible **displaying the gradient according to the number of the sub pixels Ps used as one** . If the data specifically memorized by Da and the memory Mbn in the data memorized by the memory Man is set to Db, and white shall be displayed for black at the time of 0 when said data is 1, The three sub pixels Ps are black, Da=0, and Db=1 in Da=Db=1, and, in the one sub pixel Ps, the three sub pixels Ps serve as **the two sub pixels Ps** white by black, Da=1, and Db=0 black, Da=0, and Db=0. Therefore, the display of 4 gradation is attained using the three sub pixels Ps. That is, according to this pixel configuration, as compared with a 1st embodiment, it becomes possible to make the gradation number per **in the 2nd mode** sub pixel Ps increase.

0066

The timing chart which drawing 17 is a circuit diagram showing the composition of the scanning line driving circuit 100B, and shows operation of a liquid crystal device **in / in drawing 18 / the 1st mode** , The timing chart and drawing 20 in which operation of a liquid crystal device **in / in drawing 19 / the write period in the 2nd mode** is shown are a timing chart which shows operation of the liquid crystal device in the read-out period in the 2nd mode. In drawing 17 - drawing 20, it explains here by the case where the representative circuit schematic of drawing 16 is set to n= 1.

0067

If the scanning line 2 is chosen one by one in order of signal Gc1, Gc2, and -- in the 1st mode and the signal G1, G2, and -- become active one by one, in the period t1, a signal level (the "1st line signal" in drawing 18) will be written in the sub pixels Ps (m, 1) and Ps (m+1, 1). In the period t2 following this, a signal level (the "2nd line signal" in drawing 18) is written in the sub pixels Ps (m, 2) and Ps (m+1, 2), and a signal level (the "3rd line signal" in drawing 18) is further written in the sub pixels Ps (m, 3) and Ps (m+1, 3) in the period t3. In the 1st mode, the signal Gmon (1, 1), the signal Gmon (1, 2), and the signals Gmon (1, 3) and Gmon (1, 4) serve as a low level, and each memory and each sub pixel Ps are separated.

0068

Next, in the write period in the 2nd mode, since signal Gmon2 is set to a low level while signal Gmon1 becomes high-level, as shown in drawing 19, TFT60 will be in an ON state and TFT61 will be in an OFF state. And in the period t2, t3, and --, signal Gmrw1, Gmrw2, and -- become active one by one. Therefore, the data impressed to Sm and Sm+1 in the period t2 is written in memory Ma1 and Mb1, respectively, and the data impressed to Sm and Sm+1 in the period t3 is written in memory Ma2 and Mb2, respectively.

0069

Next, in the read-out period in the 2nd mode, the Y clock signal CKY is not supplied but the scanning line driving circuit 100B suspends operation. For this reason, signal Gc1, Gc2, and -- are set to a low level, and the signal G1, G2, and -- become high-level. On the other hand, signal Gmon1 and signal Gmon2 are reversed with the 1 field period 1V. While the voltage of the capacity 62 is written in each sub pixel Ps since signal Gmon1 becomes active if it is in the period T4, since signal Gmon2 becomes active in the period T5, the voltage which reversed the voltage of the capacity 62 is written in each sub pixel Ps. It becomes possible to reverse the voltage impressed to a liquid crystal by this.

0070

According to liquid crystal panel AA of a 2nd embodiment, power consumption can be substantially reduced by **which both change the 1st mode and the 2nd mode to a display image according to** ** ****** the ability to make the number of gradients increase in the 2nd mode, without degrading the imaging quality seen from the user.

0071

<3. application>

<3-1: >, such as composition of an element substrate

In each embodiment mentioned above, the field which carries the memories Ma and Mb

in a part of picture element region A, and the field which allocated only the sub pixel Ps may be provided. especially -- the 2nd mode -- low -- what is necessary is just to arrange the main pixel P into the portion for which a minute display is sufficient
While transparent insulating substrates, such as glass, constitute the element substrate 151 of liquid crystal panel AA and forming a silicon thin film on the substrate concerned in each embodiment mentioned above, Although TFT by which the source, the drain, and the channel were formed on the thin film concerned explained as what constitutes the element of the switching element of a pixel, the data line driving circuit 200, and the scanning line driving circuits 100A and 100B, this invention is not restricted to this. This invention is applicable to the liquid crystal panel in which all the peripheral circuits required for the drive of a liquid crystal panel were formed on the element substrate, using TFT. This invention is applicable not only to said peripheral circuit but the liquid crystal panel in which a microprocessor, a memory, an interface circuit, a converter, a timing generator, an image processing circuit, etc. were formed on the element substrate. such technology is called "system one glass (System on glass)" or "system LCD."

0072

For example, a semiconductor substrate may constitute the element substrate 151 and the insulated gate field effect transistor by which the source, the drain, and the channel were formed in the surface of the semiconductor substrate concerned may constitute the switching element of a pixel, and the element of various kinds of circuits. Thus, since it cannot use as a transmission type display panel when a semiconductor substrate constitutes the element substrate 151, the picture element electrode 6 will be formed with aluminum etc., and it will be used as a reflection type. The picture element electrode 6 may only be used as a reflection type by using the element substrate 151 as a transparent base.

0073

If it was in the embodiment mentioned above, the switching element of the pixel was explained as 3 terminal elements represented with TFT, but it may constitute from 2 terminal elements, such as a diode. However, in using 2 terminal elements as a switching element of a pixel, while forming the scanning line 2 in one substrate and forming the data line 3 in the substrate of the other, it is necessary to form 2 terminal elements between either one of the scanning line 2 or the data line 3 and a picture element electrode. In this case, a pixel will comprise a one terminal pair network element by which the series connection was carried out between the scanning line 2 and the data line 3, and a liquid crystal.

0074

Although this invention was explained as an active matrix type liquid crystal display device, it is not restricted to this but can be applied also to the PASSHIIBU type using a STN (Super Twisted Nematic) liquid crystal etc. As electrooptic material, an organic light emitting diode (OLED) element or an electroluminescence (EL) element other than a liquid crystal, etc. can be used, and it can apply also to the display device which displays according to the electrooptic effect.

0075

Composition of a pixel of an electrooptics panel which used an organic light emitting diode element is shown in drawing 21 as an example. It is the following points that main pixel P' shown in drawing 21 is different from the main pixel P shown in drawing 2. A point of having formed the current supply source line 80 for supplying current to the OLED elements 73 and 75 in the 1st, It is the point of 2nd having lost a point of having formed TFT72 of a P channel, 74, and the OLED elements 73 and 75 instead of the storage capacitance 52 and 55 and the liquid crystal capacity 53 and 56, and a system controlled by Gmon2 by the 3rd. If those gate voltage is set to a low level, TFT72 and 74 will be in an ON state, and will supply current to the OLED elements 73 and 75 from the current supply source line 80. Thereby, while one, the sub pixel Ps turns off the sub pixel Ps, if TFT72 and 74 are turned off. By this, gradation will be controlled in binary. Since an OLED element is driven by DC, the number of ** without the necessity of carrying out polarity reversals unlike a case where a liquid crystal is driven, and the signals Gmon which control connection between a memory and a sub circuit for this reason is one

sufficient.

0076

The embodiment mentioned above is applicable to a plasma display etc. That is, this invention is applicable to the liquid crystal device mentioned above and all the electro-optic devices which have similar composition.

0077

<3-2: Electronic device >

<3-2-1:mobile type computer>

Next, the example which applied this liquid crystal panel AA to the mobile type personal computer is explained. Drawing 22 is a perspective view showing the composition of this personal computer. In the figure, the computer 1200 comprises the body part 1204 provided with the keyboard 1202, and the liquid crystal display unit 1206. This liquid crystal display unit 1206 is constituted by adding a back light to the back of the liquid crystal panel 1005 described previously.

0078

<3-2-3: Cellular-phone >

The example which applied this liquid crystal panel AA to the cellular phone is explained. Drawing 23 is a perspective view showing the composition of this cellular phone. In a figure, the cellular phone 1300 is provided with the reflection type liquid crystal panel 1005 with two or more manual operation buttons 1302. If it is in this reflection type liquid crystal panel 1005, a front light is provided in that front face if needed.

0079

Besides an electronic device explained with reference to drawing 22 and drawing 23, a liquid crystal television, ****** provided with a video tape recorder of a view finder type and a monitor direct viewing type, a car navigation device, pager, an electronic notebook, a calculator, a word processor, a workstation, a TV phone, a POS terminal, and a touch panel etc. are mentioned. And it cannot be overemphasized that can apply to these various electronic equipment.

Brief Description of the Drawings

Drawing 1 It is a block diagram showing the entire configuration of the liquid crystal device concerning a 1st embodiment of this invention.

Drawing 2 It is a circuit diagram showing the detailed composition of the main pixel P formed in the equipment corresponding to intersection with scanning line 2-n1 - 2-n6, data-line 3-m, and 3-m+1.

Drawing 3 It is a key map for explaining the relation between the main pixel P in the equipment, and the sub pixel Ps.

Drawing 4 It is a block diagram showing the composition of the scanning line driving circuit 100A of the equipment.

Drawing 5 It is a circuit diagram showing the composition of unit shift circuit Ua2n-1 of the scanning line driving circuit 100A of the equipment - Ua2n+1, and Logical unit Ubn.

Drawing 6 It is a circuit diagram showing the composition of the data line driving circuit 200 of the equipment.

Drawing 7 It is a timing chart of the various signals in the 1st mode of the equipment.

Drawing 8 It is a key map showing the flow of the signal of the write period in the 1st mode of the equipment.

Drawing 9 It is a timing chart which shows operation of the write period in the 2nd mode of the equipment.

Drawing 10 It is a key map showing the flow of the signal of the write period in the 2nd mode of the equipment.

Drawing 11 It is a timing chart which shows operation of the read-out period in the 2nd mode of the equipment.

Drawing 12 It is a key map showing the flow of the signal of the read-out period in the 2nd mode of the equipment.

Drawing 13 It is a perspective view explaining the composition of liquid crystal panel AA of the equipment.

Drawing 14 It is a partial sectional view for explaining the structure of liquid crystal panel AA of the equipment.
Drawing 15 It is a key map showing the pixel configuration of the liquid crystal device concerning a 2nd embodiment.
Drawing 16 It is a circuit diagram showing the detailed composition of the pixel of the equipment.
Drawing 17 It is a circuit diagram showing the composition of the scanning line driving circuit 100B of the equipment.
Drawing 18 It is a timing chart which shows the operation in the 1st mode of the equipment.
Drawing 19 It is a timing chart which shows operation of the write period in the 2nd mode of the equipment.
Drawing 20 It is a timing chart which shows the operation in the read-out period in the 2nd mode of the equipment.
Drawing 21 It is a circuit diagram showing an example of the pixel configuration of the electrooptics panel using an OLED element.
Drawing 22 It is a perspective view showing the composition of an example slack personal computer of the electronic device which applied liquid crystal panel AA.
Drawing 23 It is a perspective view showing the composition of an example slack cellular phone of the electronic device which applied liquid crystal panel AA.
Explanations of letters or numerals
AA **-- The data line, 6 / -- Picture element electrode,** -- A liquid crystal panel, A -- A picture element region, 2 -- A scanning line, 3 50 -- TFT (switching element), 100A, 100B -- Scanning line driving circuit, 200 .... A data line driving circuit, Ps -- The sub pixel Ps, P -- Main pixel, 50 **-- Capacity, 63, 64 / -- An inverter (the 1st and 2nd inverting circuit), 65 / -- TFT (the 4th switching element).** -- TFT (the 1st switching element), 60 -- TFT (the 2nd switching element), 61 -- TFT (the 3rd switching element), 62

For drawings please refer to the original document.
